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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,862	07/15/2003	H. Peter Anvin	TRAN-P082	9139

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,862	ANVIN ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003 and 20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Application on 07/15/2003 and Declaration on 01/20/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-8 and 19-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Reilly et al., U.S. Patent No. 6,925,552 (Herein referred to as Reilly).

5. Referring to claim 1, Reilly has taught a method providing partial speculative operation in lieu of suspending speculation, said method comprising:

operating in a first mode of speculative operation *(executing program instructions outside of an exception handler; column 4, lines 45-58)*, said first mode permitting speculation of a first set of speculative operations *(including at least branch, load, and store operations; column 5, lines 1-23)*; and

exiting said first mode and entering a second mode of speculative operation *(executing speculative exception handler; column 5, lines 1-23)* in response to an event *(a performance critical exception)*, said second mode permitting speculation of a second set of speculative operations that is a subset of said first set (*branch, load, and store operations; column 5, lines 1-23*).

6. Referring to claim 2, Reilly has taught the method of Claim 1 wherein said first set of speculative operations comprises microprocessor register operations *(load instructions, which load data from memory into a register; See column 5, lines 19-23)*, operations that involve memory that is private to a microprocessor *(Registers are memory that is private to the microprocessor. Therefore, register operations involve memory that is private to the microprocessor)*, input/output (I/O) writes *(store instructions, which write data to memory, an I/O device; See column 5, lines 19-23)*, main memory reads *(store instructions; See column 5, lines 1-23)*, main memory writes *(load instructions; See column 5, lines 1-23)*, and non-architectural faults *(a fault (e.g. load/store order trap) that is not genuine; See column 5, lines 11-23)*.

7. Referring to claim 3, Reilly has taught the method of Claim 1 wherein said second set of speculative operations comprises microprocessor register operations *(load instructions, which load data from memory into a register; See column 5, lines 19-23)*, operations that involve memory that is private to a microprocessor *(Registers are memory that is private to the microprocessor. Therefore, register operations involve memory that is private to the*

microprocessor), and architectural faults *(a fault (e.g. load/store order trap) that is genuine; See column 5, lines 11-23)*

8. Referring to claim 4, Reilly has taught the method of Claim 1 wherein said second set of speculative operations comprises speculative operations that are invisible external to a microprocessor *(The second set of speculative operations includes exception handler operations. Since these operations are not part of the program being executed, they are invisible external to a microprocessor; See column 5, lines 1-23)*.

9. Referring to claim 5, Reilly has taught the method of Claim 1 wherein said event is selected from the group consisting of a fault *(load/store order trap; See column 5, lines 11-23)*, a direct memory access request, and an I/O read.

10. Referring to claim 6, Reilly has taught the method of Claim 1 further comprising suspending speculative operation in response to a second event *(a non-critical exception; column 6, lines 7-29)*.

11. Referring to claim 7, Reilly has taught the method of Claim 1 further comprising returning to said first mode *(executing program instructions outside of an exception handler)* after said event is handled *(execution is returned to program instructions outside of an exception after the exception event is handled; column 6, lines 7-29)*.

12. Referring to claim 8, Reilly has taught the method of Claim 1 further comprising:

counting the number of instructions executed in said first mode prior to said event *(The number of instructions is counted using the program counter, which is inherently needed to correctly execute the program)*; and

returning to said first mode upon executing the same number of instructions after entering said second mode *(Since the excepting instruction is executed (section 3.1 on pages 3-4), at least the same number of instructions are executed)*.

13. Referring to claim 19, Reilly has taught a computer system comprising:

a main memory *(Inherent for operation of load/store instructions since load/store instructions require reading/writing to a main memory; column 5, lines 11-23)*; and

a microprocessor *(Fig. 1. component 50)* coupled to said main memory *(Since the microprocessor executes said load/store instructions it is inherently coupled to the main memory)*;

wherein said computer system implements a first mode of speculative operation *(executing program instructions outside of an exception handler; column 4, lines 45-58)*, a second mode of partial speculative operation *(executing speculative exception handler; column 5, lines 1-23)*, and a third mode *(executing non-speculative exception handler; column 5, lines 1-23)* in which speculative operations are suspended in entirety *(The non-speculative exception handler only handles non-speculative exceptions, therefore all speculative operations are suspended while executing the non-speculative exception hander -column 6; lines 7-29)*.

14. Referring to claim 20, given the similarities between claim 2 and claim 20 the arguments as stated for the rejection of claim 2 also apply to claim 20.

15. Referring to claim 21, given the similarities between claim 3 and claim 21 the arguments as stated for the rejection of claim 3 also apply to claim 21.

16. Referring to claim 22, given the similarities between claim 4 and claim 22 the arguments as stated for the rejection of claim 4 also apply to claim 22.

17. Referring to claim 23, given the similarities between claim 5 and claim 23 the arguments as stated for the rejection of claim 5 also apply to claim 23.

18. Referring to claim 24, given the similarities between claim 7 and claim 24 the arguments as stated for the rejection of claim 7 also apply to claim 24.

19. Referring to claim 25, given the similarities between claim 8 and claim 25 the arguments as stated for the rejection of claim 8 also apply to claim 25.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 9 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reilly in view of Dehnert et al., "The Transmeta Code Morphing Software: Using Speculation, Recovery, and Adaptive Retranslation to Address Real-Life Challenges" (Herein referred to as Dehnert).

22. Referring to claim 9, Reilly has taught the method of Claim 1 implemented using a microprocessor comprising host hardware *(column 4, lines 45-58)*.

Reilly does not disclose expressly that the microprocessor additionally comprises translation software, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions into a sequence of native instructions, wherein said interpreting is permitted during said second mode.

Dehnert discloses a microprocessor *(Transmeta Crusoe microprocessor)* comprising a combination of translation software *(Code Morphing Software (CMS); See Fig. 1)* and host hardware *(VLIW processor; See second paragraph of section labeled "Crusoe and CMS" on page 2)*, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions *(x86 instructions)* into a sequence of native instructions (VLIW instruction "molecule"), wherein said interpreting is permitted during exception handling *(Dehnert; See section labeled "Crusoe and CMS" on pages 2-3)*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the microprocessor of Reilly to include translation software that interprets and translates a sequence of non-native instructions into a sequence of native instructions, wherein said interpreting is permitted during exception handling, as taught by Dehnert.

The suggestion/motivation for doing so would have been that translation software allows the native instruction set to be modified while the microprocessor

advantageously remains compatible with programs written using the non-native instructions *(Dehnert; See section labeled "Crusoe and CMS" on pages 2-3)*.

Therefore, it would have been obvious to combine Dehnert with Reilly to obtain the invention as specified in claim 9.

23. Referring to claim 26, given the similarities between claim 9 and claim 26 the arguments as stated for the rejection of claim 9 also apply to claim 26.

24. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dehnert in view of Reilly.

25. Referring to claim 10, Dehnert has taught a method providing partial speculative operation, said method comprising:

executing forward from a speculation boundary *(start of a translation)* representing a memory state *(shadow register state)*, said executing according to a full speculation mode that permits a set of speculative operations *(See section 3.1 on pages 3-4)*;

experiencing an event *(exception)* during said executing *(See section 3.1 on pages 12-13)*;

rolling back to said speculation boundary *(start of a translation)* and restoring said memory state *(shadow register state)* in response to said event *(See section 3.1 on pages 3-4)*;

executing forward from said speculation boundary non-speculatively *(Execution from speculation boundary is done in-order and therefore non-speculatively; See section 3.1 on pages 3-4)*

Dehnert does not disclose expressly that executing forward from said speculation boundary is done according to a partial speculation mode that permits a subset of said set of speculative operations, said partial speculation mode used in lieu of suspending said set of speculative operations in entirety.

Reilly discloses executing according to a partial speculation mode *(Reilly; executing speculative exception handler; column 5, lines 1-23)* that permits a subset *(Reilly; branch, load, and store operations; column 5, lines 1-23)* of the set of speculative operations, said partial speculation mode used in lieu of suspending said set of speculative operations in entirety.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Dehnert to execute forward from a speculation boundary according to a partial speculation mode that permits a subset of the set of speculative operations as taught by Reilly.

The suggestion/motivation for doing so would have been that the quicker resolution of exceptions is advantageously permitted and program execution is not delayed *(Reilly; column 3, lines 63-65)*.

Therefore, it would have been obvious to combine Reilly with Dehnert to obtain the invention as specified in claim 10.

26. Referring to claim 11, Dehnert and Reilly have taught the method of Claim 10 wherein said set of speculative operations comprises microprocessor register

operations *(Dehnert; Since registers are shadowed, register operations must execute speculatively; see second paragraph of section 3.1)*, operations that involve memory that is private to a microprocessor *(Registers are memory that is private to the microprocessor. Therefore, register operations involve memory that is private to the microprocessor)*, input/output (I/O) writes *(Dehnert; see fourth paragraph of section 3.4)*, main memory reads *(Dehnert; see second paragraph of section 3)*, main memory writes *(Dehnert; see second paragraph of section 3)*, and non-architectural faults *(Dehnert; faults (i.e. errors) that are not genuine; see section 3.2)*.

27. Referring to claim 12, Dehnert and Reilly have taught the method of Claim 10 wherein said subset of speculative operations comprises microprocessor register operations *(Reilly; load instructions, which load data from memory into a register; See column 5, lines 19-23)*, operations that involve memory that is private to a microprocessor *(Registers are memory that is private to the microprocessor. Therefore, register operations involve memory that is private to the microprocessor)*, and architectural faults *(Reilly; a fault (e.g. load/store order trap) that is genuine; See column 5, lines 11-23)*.

28. Referring to claim 13, Dehnert and Reilly have taught the method of Claim 10 wherein said subset of speculative operations comprises speculative memory operations that are invisible external to a microprocessor *(Reilly: The second set of speculative operations includes exception handler load/store (i.e. memory) operations. Since these operations are not part of the program being executed, they are invisible external to a microprocessor. See column 5, lines 1-23)*.

29. Referring to claim 14, Dehnert and Reilly have taught the method of Claim 10 wherein said event is selected from the group consisting of a fault *(Dehnert; see section 3.2)*, a direct memory access request, and an I/O read.

30. Referring to claim 15, Dehnert and Reilly have taught the method of Claim 10 further comprising:

detecting a second event during operation in said partial speculation mode *(Reilly; a non-critical exception)*; and

suspending speculative operation in response to said second event ; *(Reilly; When the non-critical exception is determined to reside in the actual program path speculative operation is suspended and the exception is handled; column 6, lines 7-29).*

31. Referring to claim 16, Dehnert and Reilly have taught the method of Claim 10 further comprising:

handling said event *(Reilly; executing speculative exception handler; column 5, lines 1-23)*; and

returning to said full speculation mode after said event is handled *(Reilly; execution is returned to program instructions outside of an exception after the exception event is handled; column 6, lines 7-29).*

Referring to claim 17, Dehnert and Reilly have taught the method of Claim 10 further comprising:

counting the number of instructions executed in said full speculation mode prior to said event *(The number of instructions is counted using the program counter, which is inherently needed to correctly execute the program)*;

executing the same number of instructions after entering said partial speculation mode *(Dehnert; The instructions corresponding to the faulting translation are executed. Therefore, at least the same number of instructions are executed; See section 3.1 on pages 3-4)*; and

returning to said full speculation mode after executing said same number of instructions *(Dehnert; See section 3.1 on pages 3-4)*.

32. Referring to claim 18, Dehnert and Reilly have taught the method of Claim 10 implemented using a microprocessor comprising a combination of translation software and host hardware, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions into a sequence of native instructions, wherein said interpreting is permitted during said partial speculation mode *(Dehnert; See section 2 on pages 2-3)*.

Conclusion

33. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Klaiber, "The Technology Behind Crusoe Processors", teaches a microprocessor comprising translation software that uses shadow registers to recovery from exceptions.

Altman et al., "BOA: The Architecture of a Binary Translation Processor", teaches a microprocessor comprising translation software.

Hwu et al., "Checkpoint Repair for Out-of-order Execution Machines", teaches using checkpoints to recover from exceptions.

Babaian et al., U.S. Patent Application No. 2002/0092002, teaches preserving precise exceptions in a system comprising translation software.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

2/6/06

HENRY W. H. TSAI
PRIMARY EXAMINER